Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claim 1 (*Currently Amended*): A transceiver system comprising:

a plurality of transceiver chips, each transceiver chip having a plurality of serializer/deserializer (SERDES) cores, each SERDES core having one or more SERDES lanes, each SERDES lane having a receive channel and a transmit channel,

wherein the transmit channel of each SERDES lane is phase-locked with a corresponding receive ~~channel of a different SERDES lane than that of the transmit channel~~ channel; and

wherein the transmit channel is part of a first SERDES lane of a first SERDES core, and the corresponding receive channel is part of a second SERDES lane of a second SERDES core.

Claim 2 (*Currently Amended*): The transceiver system of claim 1, wherein each SERDES core is configured to receive and transmit ~~receives and transmits~~ data to and from external components connected to the SERDES core.

Claim 3 (*Original*): The transceiver system of claim 2, wherein the external components include disk drives.

Claim 4 (*Previously Cancelled*)

Claim 5 (*Cancelled*)

Claim 6 (*Cancelled*)

Claim 7 (*Currently Amended*): The transceiver system of claim [[6]] 1, wherein the first SERDES core and the second SERDES core are disposed on a common substrate.

Claim 8 (*Currently Amended*): The transceiver system of claim [[6]] 1, wherein the first SERDES core is disposed on a first substrate and the second SERDES core is disposed on a second substrate.

Claim 9 (*Original*): The transceiver system of claim 8, wherein the first substrate and the second substrate are disposed on a common board.

Claim 10 (*Original*): The transceiver system of claim 8, wherein the first substrate is disposed on a first board and the second substrate is disposed on a second board.

Claim 11 (*Original*): A method of transferring data from a first external component coupled to an active receive channel of a transceiver system to a second external component coupled to an active transmit channel of the transceiver system, in which a transmit clock signal of the active transmit channel is phase-locked with a receive clock signal of the active receive channel, the transceiver system comprising a plurality of transceiver chips, each transceiver chip having a plurality of serializer/deserializer (SERDES) cores, each SERDES core having one or more SERDES lanes, each SERDES lane having a receive channel and a transmit channel, the method comprising:

receiving, at the active receive channel, external component data from the first external component;

transferring the external component data and receive clock phase data from the active receive channel to the active transmit channel;

phase-locking the transmit clock signal with the receive clock signal per the receive clock phase data; and

transmitting, from the active transmit channel, the external component data to the second external component.

Claim 12 (*Original*): The method of claim 11, wherein the first and second external components include disk drives.

Claim 13 (*Original*): The method of claim 11, wherein:

the receiving step receives the external component data in analog format;

the transferring step transfers the external component data and receive clock signal phase data in digital format; and

the transmitting step transmits the external component data in analog format.

Claim 14 (*Original*): The method of claim 11, wherein:

the receiving step receives the external component data in series;

the transferring step transfers the external component data and receive clock signal phase data in parallel; and

the transmitting step transmits the external component data in series.

Claim 15 (*Original*): The method of claim 11, wherein the active transmit channel and the active receive channel are each part of a common SERDES lane.

Claim 16 (*Original*): The method of claim 11, wherein the active transmit channel is part of a first SERDES lane of a common SERDES core, and the active receive channel is part of a second SERDES lane of the common SERDES core.

Claim 17 (*Original*): The method of claim 11, wherein the active transmit channel is part of a first SERDES lane of a first SERDES core, and the active receive channel is part of a second SERDES lane of a second SERDES core.

Claim 18 (*Original*): The method of claim 17, wherein the first SERDES core and the second SERDES core are disposed on a common substrate.

Claim 19 (*Original*): The method claim 17, wherein the first SERDES core is disposed on a first substrate and the second SERDES core is disposed on a second substrate.

Claim 20 (*Original*): The method of claim 19, wherein the first substrate and the second substrate are disposed on a common board.

Claim 21 (*Original*): The method of claim 19, wherein the first substrate is disposed on a first board and the second substrate is disposed on a second board.